Amendments to the Specification

The paragraph on page 4, beginning on line 17:

FIG. 1 is a block diagram that illustrates communication device 100 in an example of the invention. Those skilled in the art will appreciate that some conventional aspects of communication device 100 have been omitted for the sake of clarity. Communication device 100 comprises network layer system 110, link layer system 120 and physical layer system 130. Network layer system 110 exchanges packets with link layer system 120 over connection 111. Link layer system 120 exchanges packets with physical layer system 130 over connection 131. Physical layer system 130 exchanges packets with communication path 132.

B1

The paragraph on page 4, beginning on line 29:

Link layer system 120 operates at layer two of the OSI protocol reference model. Link layer system ~~110~~ 120 handles the individual links that are used by network layer system 110. Link layer system 120 exchanges the packets between the links and the physical layer system 130 for the links.

B2

The paragraph on page 5, beginning on line 8:

Link layer system 120 includes a memory that buffers the packets during transfer. Link layer system 120 generates status signal 121 that indicates the available space in the memory. Link layer system 110 transfers status signal 121 to network layer system 110. Network layer system 110 processes status signal 121 to determine when to transfer the packets to link layer system 120. Thus, network layer system 110 can use status signal 121 to optimize performance by avoiding over-run and under-run conditions in the layer two memory.

B3

The paragraph on page 5, beginning on line 27:

FIG. 2 is a block diagram that illustrates link layer system 120 in an example of the invention. Those skilled in the art will appreciate that some conventional aspects of link layer system 120 have been omitted for the sake of clarity. Link layer system 120 comprises link layer controller 220 and memory 228. Link layer controller 220 comprises network layer interface 222, memory controller 224, and physical layer interface 226.

B4

The paragraph on page 7, beginning on line 3:

FIG. 3 is a block diagram that illustrates router 300 in an example of the invention. Those skilled in the art will appreciate that some conventional aspects of router 300 have been omitted for the sake of clarity. Router 300 comprises link layer controller 320 and Random Access Memory (RAM) 328 that are coupled by connection 345. Router 300 also comprises the following components and connections. Host processor 340 and host database 341 are coupled to each other and to link layer controller 320 by Peripheral Connect Interface (PCI) bus 343. Network processor 342 is coupled to link layer controller 320 by packet exchange bus 344. Link layer controller 320 is coupled to broadband mux 350 and framers 351-352 by respective connections 354-356. Broadband mux 350 and framers 351-352 are coupled to optical mux 353 by respective connections 357-359. Optical mux 353 is coupled to optical communication path 360. Link layer controller 320 shares expansion bus 361 with broadband mux 350, framers 351-352, and optical mux 353.

The paragraph on page 8, beginning on line 3:

Link layer controller 320 has a bandwidth of 1.6 Gigabits/second and is implemented in a low-power 1.8 volt CMOS integrated circuit. Link layer controller 320 remains operational without RAM 328. Link layer controller 320 can support multiple protocols: high-level data link control, synchronous data link control, link access procedure balanced, integrated services digital network D-channel, link access procedure D, digital multiplexed Interface, X.25, frame relay, high-speed serial interface, switched mega-bit data service, asynchronous transfer mode, and data exchange interface.

The paragraph on page 8, beginning on line 11:

Peripheral Connect Interface (PCI) bus 343 uses a PCI 2.1 interface with a 32 bit multiplexed address/data bus operating at 33 MHz or 66 MHz. Host processor 340 and host database 341 configure link layer controller 320 using PCI bus 343. Configuration includes the dynamic activation and deactivation of channels. Network processor 342 exchanges data with link layer controller 320 over packet exchange bus ~~342~~ 344.

The paragraph on page 10, beginning on line 17:

Link layer controller 320 comprises the following components and connections. ~~PCI bus~~ interface 470 is coupled to PCI bus 343. Expansion bus interface 471 is coupled to expansion bus 361 and can bridge devices onto PCI bus 343. Packet exchange bus interface ~~372~~ 472 is coupled to packet exchange bus 344 and to memory controller 424. Memory controller 424 is connected to Direct Memory Access (DMA) 473. DMA 473 is connected to receive line processor 474 and transmit line processor 475. Receive line processor 474 and transmit line processor 475 are connected to serial interface 476 which is coupled to connections 354-356.

The paragraph on page 11, beginning on line 4:

Memory controller 424 generates a transmit buffer status signal to indicate available space for each transmit buffer in DRAM 480. Memory controller ~~224~~ 424 transfers the transmit buffer status signal status signal to packet exchange bus interface 472 which transfers the transmit buffer status signal from link layer controller 320 to network processor 342 over packet exchange bus 344. Network processor 342 processes the transmit buffer status signal to control the transfer of the packets over the HDLC channels to link layer controller 320. Such control includes preventing over-run and under-run in DRAM 480.